

DATARAM

The Best Choice in Memory

Chipkill™ Memory

Advanced ECC Technology

Chipkill Memory is a new advanced ECC (Error Checking and Correcting) memory technology that protects systems from any single memory chip failure and any number of multi-bit errors from any portion of a single memory chip. The advantage of Chipkill is that it reduces system downtime and improves overall system reliability.

Background

One of the early forms of error checking technologies used during the early 1990s was parity. Parity memory can detect errors but cannot correct them. If a parity error occurs in a server, the system will crash and all of the data stored in memory will be lost.

Since even sporadic system crashes are unacceptable for servers the industry adopted ECC memory. ECC memory can detect and correct single-bit errors, and can detect but not correct double-bit errors. If more than two data bits are in error on the same access they are unlikely to be detected. All multi-bit errors, whether detected or not, are fatal and result in system downtime. Because the likelihood of multiple-bit errors is rare, ECC memory provides a good level of reliability and is standard technology today on almost every server.

Memory Errors

Memory errors are usually classified as either soft or hard. Soft errors are impermanent and are usually caused by charged particles from naturally occurring background radiation or cosmic rays. Hard errors can be caused by defects within the DRAM package among other reasons, and are usually permanent once they appear.

Most of today's DIMMs (Dual Inline Memory Modules) are built with nine or eighteen DRAM (Dynamic Random Access Memory) chips. In years past, these DRAM chips contained a single data bit. If a DRAM chip were to develop a hard error, it would affect only a single data bit and would be detected and corrected by the ECC circuitry. However, to obtain the highest capacity DIMMs today, the DRAM chips must contain as many bits as possible—usually four, eight, or sixteen. If one of these DRAM chips were to develop a hard error, the likelihood of it affecting more than a single bit is increased. A simple Hamming type ECC cannot recover the four, eight, or sixteen bits of data, producing a fatal error and system downtime. Today's dense DIMMs are also more likely to sustain multiple bit errors when bombarded by charged particles or cosmic rays. Standard ECC technology, which was highly reliable just a few years ago, is quickly becoming insufficient for today's servers.

Chipkill

Chipkill is an advanced form of ECC that has the ability to withstand a multi-bit failure within a DRAM chip, including a failure that would affect all data bits, whether that is four, eight, or sixteen.

Figure 1 shows how data is organized on a typical double-sided 512MB DIMM using standard ECC. Eight ECC bits are assigned per sixty-four bits of data.

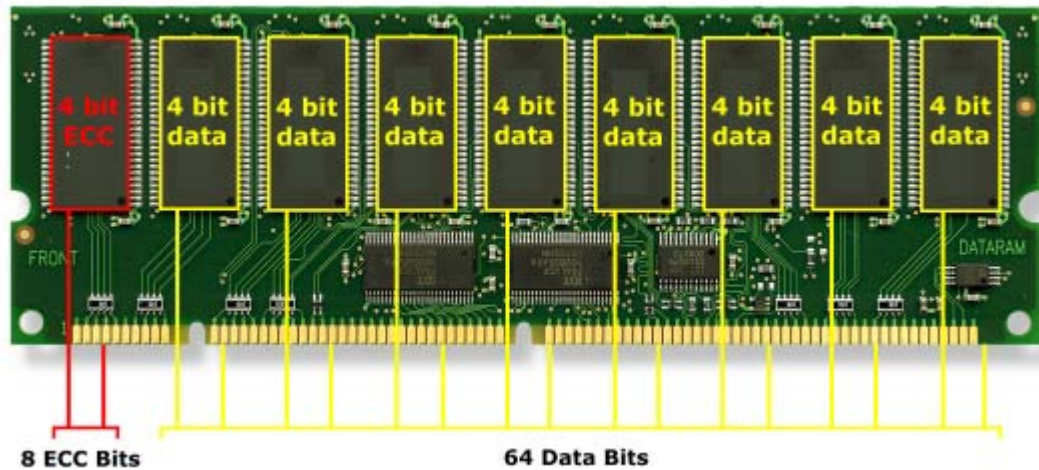


Figure 1

Chipkill can be implemented using several methods. The most common form involves memory interleaving and "bit scattering."

A typical memory system can be designed to use 256 data bits (or four 64-bit "words"). To do this, DIMMs must be installed in groups of four and be identical in configuration and capacity. ECC bits are included so that the entire width of data and ECC bits is 288 (four 72-bit DIMMs provides 288 total bits). Stopping at this point would provide standard ECC protection. However, by scattering bits, Chipkill protection emerges.

Figure 2 shows how the four words, each consisting of 64 data bits and 8 ECC bits, are scattered.

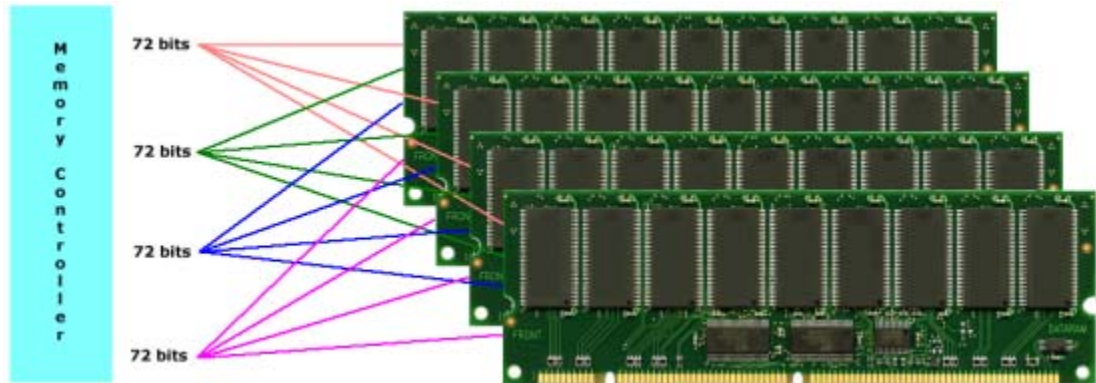


Figure 2

Figure 3 shows how a four-bit DRAM chip on one of the DIMMs has its four bits scattered into separate words. If a failure occurs that causes all four bits of a DRAM chip to be in error, no single word will experience more than a single bit of bad data—a situation that can be detected and corrected.

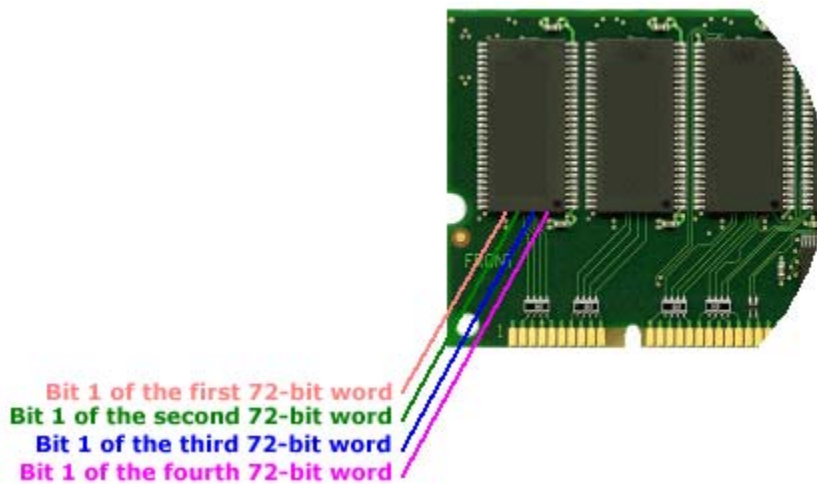


Figure 3

In addition bit scattering, another method would be to design a memory system that provided more ECC bits so that more than a single bit failure could be corrected. A combination of both methods could be used to provide Chipkill support when using x8 and x16 DRAM chips.

Detection, Correction, and Reporting

The detection, correction, and reporting of errors with Chipkill is identical to that of standard ECC. There is no server performance penalty beyond what is normal in standard ECC systems.

The actual detection, correction, and reporting of memory errors is handled by the system's chipset. A chipset consists of controller chips on a system or motherboard that control the various buses, such as the memory bus, around the CPU. Error checking codes are generated for the ECC bits during every write cycle, and checked during every read cycle. If a correctable error is uncovered, the data is automatically corrected before it is sent to whatever device had requested it. At the same time, the error is recorded and reported to the BIOS or firmware. Software management tools, often included with servers, monitor the errors and issue reports accordingly. Although a hard single-bit or Chipkill failure does not cause system downtime, it does increase the risk that any additional errors could cause a fatal, uncorrectable error that would take the server down. System administrators are advised to schedule time for service and replace degraded DIMMs.

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